ABSTRACT OF THE DISCLOSURE

A logic circuit having a self-test function includes a plurality of F/Fs having at least first-, second- and last-stage scanning F/Fs, each having a clock input, a scanning input and a scanning output terminals. The scanning F/Fs are connected one another so as to supply a scanning clock signal to the clock input terminal of each scanning F/F and a signal from the scanning output terminal of the first-stage to the scanning input terminal of the second-stage for sequential logical operations. Also provided in the logic circuit are a data selector to select either an external scanning signal or a signal output from the scanning output terminal of the last-stage and fed back through a feed-back signal line and a scanning controller to supply a control signal to the data selector so as to supply the signal fed back from the last-stage to the scanning input terminal of the first-stage, thus controlling each F/F in an internal scanning mode. The signal from the last-stage is supplied from the logic circuit via an external scanning output terminal.